WHAT IS CLAIMED IS:

1. A semiconductor memory device comprising:

a memory unit including a memory core formed by arranging a plurality of memory cells in a form of a matrix, a block as a unit having a redundant line comprising redundant cells for repairing an abnormal cell occurring in the memory core, and further one such unit block or a plurality of such unit blocks arranged in a form of a matrix;

built-in self-test means mounted on a same chip as said memory unit, for evaluating quality of each of said memory cells;

storing means mounted on the same chip as said memory unit; and

repair search means for storing in said storing means only a minimum of address pairs required to determine redundant cells for repair among address pairs in a row direction and a column direction of abnormal cells, the address pairs being sent from said built-in self-test means.

2. A semiconductor memory device as claimed in claim 1,

wherein said repair search means is provided for each said unit block.

3. A semiconductor memory device as claimed in claim 1,

wherein letting n1 be a number of redundant lines in the row direction and n2 be a number of redundant lines in the column direction, said storing means has a buffer capacity of (2 × n1 × n2) buffers as a buffer capacity for storing said address pairs.

4. A semiconductor memory device as claimed in claim 1,

wherein said repair search means has a flag indicating a number of address pairs having a row-direction address of a same value as an address pair stored in said storing means and a number of address pairs having a column-direction address of a same value as the address pair stored in said storing means; and

said repair search means determines whether the address is to be set as a final repair address on the basis of the flag.

5. A semiconductor memory device as claimed in claim 1,

wherein said repair search means has a bit for distinguishing a row-direction repair address and a column-direction repair address set as a repair address among row-direction addresses and column-direction

addresses stored in said storing means.

6. A semiconductor memory device comprising:

a memory unit including a memory core formed by arranging a plurality of memory cells in a form of a matrix, a block as a unit having a redundant line comprising redundant cells for repairing an abnormal cell occurring in the memory core, and further one such unit block or a plurality of such unit blocks arranged in a form of a matrix;

built-in self-test means mounted on a same chip as said memory unit, for evaluating quality of each of said memory cells;

storing means mounted on the same chip as said memory unit;

repair search means for storing in said storing means only a minimum of address pairs required to determine redundant cells for repair among address pairs in a row direction and a column direction of abnormal cells, the address pairs being sent from said built-in self-test means; and

built-in self-repair means mounted on the same chip as said memory unit, for calculating final repair address information of the redundant cells for repairing the abnormal cells on the basis of the address pairs stored

in said storing means.

7. A semiconductor memory device as claimed in claim 6,

wherein said memory unit has a fuse for selecting a redundant cell for repairing an abnormal cell; and said built-in self-repair means specifies said fuse on the basis of the calculated final repair address information.

8. A semiconductor memory device as claimed in claim 6,

wherein said built-in self-repair means first gives an arbitrary pattern set to all the address pairs of abnormal cells stored in said storing means, the arbitrary pattern set indicating whether repair is made by a redundant line in the column direction or whether repair is made by a redundant line in the row direction, and then determines whether repair can be made; and

when repair cannot be made, said built-in self-repair means gives a next pattern set, and when a pattern set enabling repair is found, said built-in self-repair means generates final repair address information of the redundant cells for repair on the basis of the pattern set.

9. A semiconductor memory device as claimed in claim 8,

wherein said built-in self-repair means uses a 1-bit flag, and the flag indicates whether each abnormal cell is repaired by a redundant line in the column direction or by a redundant line in the row direction.

10. A semiconductor memory device as claimed in claim 9,

wherein said 1-bit flag is provided for each address pair stored in said storing means.

11. A semiconductor memory device as claimed in claim 8,

wherein in determining whether repair can be made after giving a pattern set, said built-in self-repair means has address storing means for storing address information of redundant lines for replacing abnormal cells and determines whether said pattern set enables repair by comparing a number of pieces of address information stored in said address storing means with a number of redundant lines.

12. A semiconductor memory device as claimed in claim 7,

wherein said fuse is an electric fuse that, when a repair address is determined by said built-in self-repair means, selects a corresponding redundant cell by setting information of the repair address in the fuse.

13. A semiconductor memory device as claimed in claim 12,

wherein said electric fuse includes a register.

14. A semiconductor memory device as claimed in claim 12,

wherein a plurality of said registers are connected into a form of a chain, and the final repair address information calculated by said built-in self-repair means is transferred to the individual registers by shift operation.

15. A semiconductor memory device as claimed in claim 12,

wherein said electric fuse includes a nonvolatile memory.

16. A semiconductor memory device as claimed in claim 12,

wherein said fuse includes a mechanical fuse and an electric fuse, and one of the two fuses is selected and used.

17. A repair search method in a semiconductor memory device, said semiconductor memory device comprising:

a memory unit including a memory core formed by arranging a plurality of memory cells in a form of a

matrix, a block as a unit having a redundant line comprising redundant cells for repairing an abnormal cell occurring in the memory core, and further one such unit block or a plurality of such unit blocks arranged in a form of a matrix;

built-in self-test means mounted on a same chip as said memory unit, for evaluating quality of each of said memory cells;

storing means mounted on the same chip as said memory unit; and

repair search means for storing in said storing means only a minimum of address pairs required to determine redundant cells for repair among address pairs in a row direction and a column direction of abnormal cells, the address pairs being sent from said built-in self-test means;

wherein final repair address information of redundant cells for repairing the abnormal cells is determined for each said unit block on the basis of the address pairs stored in said storing means.

18. A repair search method as claimed in claim 17,

wherein when said redundant line is commonly used by a plurality of unit blocks in the row direction or the column direction, address information of a redundant line

for repairing an abnormal cell is determined for each of said plurality of unit blocks; and

the determined address information is given to the other unit blocks, and using the given address information, final repair address information of redundant cells for repairing abnormal cells is determined for said plurality of unit blocks.

19. A repair search method as claimed in claim 18,

wherein processing is repeated in which an address pattern set of redundant cells enabling repair is found for one of said plurality of unit blocks, the found address pattern set imposes a limitation on another unit block, an address pattern set of redundant cells enabling repair is generated for the other unit block under the limitation, and a limitation is imposed on yet another unit block on the basis of a result of the address pattern set.

20. A self-repair method in a semiconductor memory device, said semiconductor memory device comprising:

a memory unit including a memory core formed by arranging a plurality of memory cells in a form of a matrix, a block as a unit having a redundant line comprising redundant cells for repairing an abnormal cell occurring in the memory core, and further one such unit

block or a plurality of such unit blocks arranged in a form of a matrix;

built-in self-test means mounted on a same chip as said memory unit, for evaluating quality of each of said memory cells;

storing means mounted on the same chip as said memory unit; and repair search means for storing in said storing means only a minimum of address pairs required to determine redundant cells for repair among address pairs in a row direction and a column direction of abnormal cells, the address pairs being sent from said built-in self-test means;

wherein an arbitrary pattern set indicating whether repair is made by a redundant line in the column direction or whether repair is made by a redundant line in the row direction is first given to all the address pairs of abnormal cells stored in said storing means, and then whether repair can be made is determined; and

when repair cannot be made, a next pattern set is given, and when a pattern set enabling repair is found, final repair address information of the redundant cells for repair is generated on the basis of the pattern set.

21. A self-repair method as claimed in claim 20, wherein address information of redundant cells for

repairing abnormal cells is stored and whether said pattern set enables repair is determined by comparing a number of pieces of said address information stored with a number of redundant lines.

22. A self-repair method as claimed in claim 20, wherein processing for generating the address information of said redundant cells is performed when power to said semiconductor memory device is turned on.

23. A self-repair method as claimed in claim 20, wherein processing for generating the address information of said redundant cells is performed periodically or when an abnormal cell occurs.

24. A self-repair method as claimed in claim 20, wherein when said redundant line is commonly used by a plurality of unit blocks in the row direction or the column direction, each piece of address information of said plurality of unit blocks is converted into address information within one of said plurality of unit blocks, said plurality of unit blocks are superimposed on an address map to appear as one unit block, and the address information of said redundant cells is generated on the basis of the converted address information.